REMARKS

The claims remaining in this patent application following amendment are Claims 1-7 and 9-16. Original Claim 8 has been cancelled, without prejudice. Claims 11-16 are recited for the first time. Claim 1 has been amended, and original Claims 6 and 7 are objected to but are indicated to contain patentable subject matter.

Claims 1, 2, and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by the patent to Austruy, et al. (5,140,691). Independent Claim 1 has been amended to recite a peripheral bus interconnect system including first and second controllers connected to first and second peripheral bus lines, said first and second controllers including control circuitry to send health status signals to each other to indicate the normal operation of said first and second controllers, said control circuitry being responsive to the absence of a health status signal to indicate a malfunction of one of the first or second controllers, wherein the control circuitry of the normally functioning controller generates a power down signal to shut down the malfunctioning controller and a switch control signal to cause a normally open switch to close so that the first and second peripheral bus lines are connected together and to the normally functioning controller by way of the switch.

Original Dependent Claim 8 has been cancelled, and the features thereof added to Independent Claim 1, amended. As noted in the Office Action, it may be that the patent to Cebasek, et al. (6,104,963) describes a system in which surrogate device objects receive heartbeat status information from a device object to indicate whether the device object is still operational. However, this casual reference to receiving a "heartbeat" is a very long way from the applicant's

invention as recited in Independent Claim 1, amended, where the absence of such a heartbeat or health status signal causes control circuitry of a normally functioning controller to generate a power down signal to shut down a malfunctioning controller and to initiate a switch control signal by which to close a normally open switch and thereby connect the normally functioning controller to first and second peripheral bus lines via said switch. There is absolutely nothing in the teaching of Austruy, et al. to suggest that one of the processing units (26, 28) of Austruy, et al. does or would have control circuitry that is responsive to the "health status" of the other of the processing units in order to shut down a malfunctioning processing unit and generate a switch control signal. To reach a contrary result, would require a complete reinvention of Austruy, et al. in a manner that has not been contemplated or suggested by the teaching thereof.

More particularly, there is nothing in either of the patents to Cebasek, et al. or Austruy, et al. that would encourage or motivate one of ordinary skill in the art to redesign the processing units of Austruy, et al. to be able to transmit health status signals therebetween and to be responsive to the absence of a health status signal for causing a malfunctioning processing unit to be shut down and for generating a switch control signal in response to the absence of such a health status signal for also causing a normally open switch to be closed for connecting first and second peripheral bus lines together and to the normally functioning processing unit. Accordingly, Independent Claim 1, amended, is believed to recite a patentable peripheral bus interconnect system over any reasonable combination of Austruy, et al. and Cebasek, et al. Inasmuch as Independent Claim 1, amended, is believed to be patentable, each of Claims 2-7, 9 and 10 which, depend therefrom, are likewise believed to be patentable.

Claims 3-5 are rejected as being unpatentable over the aforementioned patent to Austruy, et al. (5,140,691) in view of the patents to Dixon, et al. (5,175,822) and Bell (6,678,721). Claims 3-5 depend from Independent Claim 1. Inasmuch as Independent Claim 1, amended, is believed to be patentable, Claims 3-5, which depend therefrom, are likewise believed to be patentable.

Claim 8 is rejected under 35 U.S.C. 103 as being unpatentable over the aforementioned patent to Austruy, et al. in view of the aforementioned patent to Cebasek, et al. Claim 8 has been cancelled without prejudice and, therefore, the rejection thereof is rendered moot. Nevertheless, and for the reasons stated above, Independent Claim 1, amended, which includes the features of former Claim 8, is believed to be patentable over any reasonable combination of Austruy, et al. in view of Cebasek, et al.

Claims 11-16 are recited for the first time. Newly presented Independent Claim 11 recites a peripheral bus interconnect system comprising first and second peripheral bus lines and first and second controllers, each of said first and second controllers including a switch control circuit and a bus isolator, one of said first and second controllers being powered up before the other and the switch control circuit of the first to power up controller causing a normally open switch to close temporarily so that the first to power up controller is connected to each of the first and second peripheral bus lines by way of said switch in order to assign addresses to and configure arrays of peripheral devices connected to said peripheral bus lines, and the bus isolator of said first to power up controller disconnecting said first to power up controller from said first and second peripheral bus lines following the assignment of the addresses and the configuration of said arrays of

peripheral devices connected to said first and second peripheral bus lines, whereupon the second to power up controller is connected to said first and second peripheral bus lines.

As noted in the Office Action, it may be that the patent to Dixon, et al. (5,175,822) generally describes a system having multiple controllers wherein one controller is designated to assign addresses. As also noted in the Office Action, it may further be that the patent to Bell (6,678,721) describes first powering up a master controller from a group of controllers. However, these unrelated and casual descriptions of controllers are not likely to be combined with Austruy, et al. without a complete reinvention of Austruy, et al. in a manner that has not been contemplated or suggested by the teachings thereof.

Firstly, there is absolutely no teaching in Dixon, et al. or Bell or any other patent of record of controllers which include switch control circuitry and/or a bus isolator in the manner recited by the applicant in new Independent Claim 11. Moreover, neither one of the control unit parts (26, 28) of Austruy, et al. includes a bus isolator of any kind. Any bus isolation performed by Austruy, et al. resides entirely in switch parts (38, 40) which requires that Austruy, et al. have two switch parts rather than the single switch that is shown and described by the applicant. What is still more, there is no provision or recognition in Austruy, et al. for a first to power up controller to cause a normally open switch to close and thereby connect first and second peripheral bus lines together and to said first to power up controller and for the first to power up controller to be disconnected from the first and second peripheral bus lines so that the second to power up controller can be connected to the bus lines via the switch. Therefore, there is nothing to encourage, motivate or suggest to one of

ordinary skill in the art to combine the disparate matrix of patents that is listed in the Office Action to achieve a peripheral bus system as is recited by the applicant in new Independent Claim 11. Accordingly, Independent Claim 11 is believed to be patentable over all of the patents individually and in combination which have been cited in the Office Action. Inasmuch as newly presented Independent Claim 11 is believed to be patentable, newly presented Claims 12-16, which depend therefrom, are likewise believed to be patentable.

In view of the foregoing, each of Claims 1-7 and 9-16 now appearing in this patent application is believed to recite a patentable peripheral bus interconnect system. Accordingly, reconsideration of the Examiner's rejection is requested and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

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